

8.5 256-Channel Neural Recording Microsystem with On-Chip 3D Electrodes

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Neural activity of the brain exhibits considerable heterogeneity across biological ensembles. Multi-channel neural sensory systems capture and utilize this heterogeneity. In applications such as neural prostheses, animal studies and high throughput drug screening, recordings from multiple sites within a volume of tissue are required. Recording microsystems with three-dimensional (3D) electrode arrays of various configurations have been reported such as with electrodes co-planar with the die [1]. Implementations with 3D electrode arrays bonded directly to the surface of the chip have been proposed [2]. A CMOS neural recording chip is presented with two electrode configurations, 3D golden-bump electrodes and the Utah Electrode Array (UEA), bonded directly onto the surface of the chip.

As the bandwidth of neural signals can reach above 5kHz, sensory systems that record many channels simultaneously yield large amounts of data that cannot be efficiently stored, processed or transmitted. Conventional spike detection systems [1-3] capture the majority of action potentials but discard other important neuro-physiological information such as activity below or above a threshold level, or activity in an abnormal neurological state. The presented sensory microsystem records neural activity simultaneously on 256 channels and performs analog delta compression of all recorded neural data. The output data rate is proportional to the mere information rate not the dimensions of the array or the sampling rate.

The recording channels are organized in a 16×16 array as shown in Fig. 8.5.1 (left). The 200μm cell pitch is dictated by extracellular recording spatial resolution requirements such as those in the hippocampi of mice. The non-passivated electrode bonding pads are 80×80μm² in size each. Experimentally measured characteristics are summarized in the table in Fig. 8.5.1 (right).

The recording array has been integrated with two electrode embodiments shown in Fig. 8.5.2 (top). For low penetration depth applications, 257 golden bumps, 100μm long each, such as the ones shown in Fig. 8.5.2 (top, left) were bonded onto the die. One electrode was utilized as an optional reference electrode. For higher penetration depth applications, a 10×10 Utah Electrode Array (UEA) was bonded onto the die (Fig. 8.5.2, top, right). As the 400μm UEA electrode pitch is twice the recording channel cell pitch, a set of 8×8 electrodes were bonded for a total of 64 recording sites. The bonding process is as follows. Golden stud bumps are bonded to the aluminum pads and are coined. Conductive epoxy is deposited onto the stud bumps. The array is optically aligned and placed onto the bumps. The epoxy is thermally cured. Once the die is wire-bonded, the package cavity is filled with a biocompatible epoxy in order to insulate and protect the bonding wires. The microsystem is placed into a fluidic chamber for in vitro validation (Fig. 8.5.2, bottom, left). Its functionality is validated in neurophysiological experiments (Fig. 8.5.2 bottom, right).

To preserve channel-to-channel signal coherence, each recording channel is implemented as an independent two-stage continuous time voltage amplifier depicted in Fig. 8.5.3 (top). The high-pass filter sub-Hz cut-off frequency is controlled by high-resistance sub-threshold biased MOS transistors [2]. It removes the inherent electrode-tissue interface DC offset. The cut-off frequency of the low-pass anti-aliasing filter is set by the bias current of a

transconductance amplifier. The gain is programmable and is set by re-configuring a bank of capacitors in the feedback of the second stage. Leakage-induced DC drift is removed by periodic resetting of the amplifier into the unity gain configuration [4]. An example of a recording of chemically induced seizure-like activity in an intact hippocampus of a mouse through an on-chip UEA electrode is shown in Fig. 8.5.3 (bottom).

The circuit diagram of the first stage amplifier and its characteristics are given in Fig. 8.5.4 (left). As the output signal swing is low, the telescopic topology is employed. It yields a factor of five reduction in power dissipation of the first stage compared to the designs in [5] and [6] for the same noise. This is due to both fewer DC signal paths and fewer sources of noise. The noise level of 7μV over 5kHz bandwidth is chosen as an acceptable tradeoff for a reduction in channel area by a factor of four over that in [5], as dictated by the cell pitch requirement. As the second stage requires a larger voltage swing, the current mirror transconductance amplifier topology is employed. The sample-and-hold circuit is implemented as a buffered analog double memory [6]. The two capacitors store two subsequent recording samples to implement delta compression as discussed below. Bottom plate sampling keeps charge injection signal-independent.

Figure 8.5.5 shows two-dimensional electrical activity data experimentally recorded on a test chip. A drop of water was placed on the surface of the 16×16 electrode array and driven by a 2mV peak-to-peak sinusoid. The stimulus signal was recorded at a 5kHz sampling rate and displayed in real time as an 'electronic video' stream. The figure shows a 3D map of the recording frame corresponding to a peak of the input sinusoid.

Delta compression is performed by thresholding the difference of two subsequent neural activity 'frames' as depicted in Fig. 8.5.6 (top). To validate the approach in high spatial resolution neural interfaces, a neural activity data set was recorded optically using a voltage-sensitive die. The delta compression algorithm was then simulated for different threshold levels. The resulting PSNR versus compression ratio trade-off is plotted in Fig. 8.5.6 (bottom).

The column-parallel switched capacitor difference circuit depicted in Fig. 8.5.7 (left) performs frame differencing during array read-out. It computes a temporal derivative of the signal as demonstrated in the experimental measurements for one channel in Fig. 8.5.7 (right). The accuracy of the output waveform presented is limited by the off-chip A/D converter resolution.

References:

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- [5] R. Harrison, C. Charles, "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications," *IEEE J. Solid-State Circuits*, vol. 38, pp. 958-965, June, 2003.
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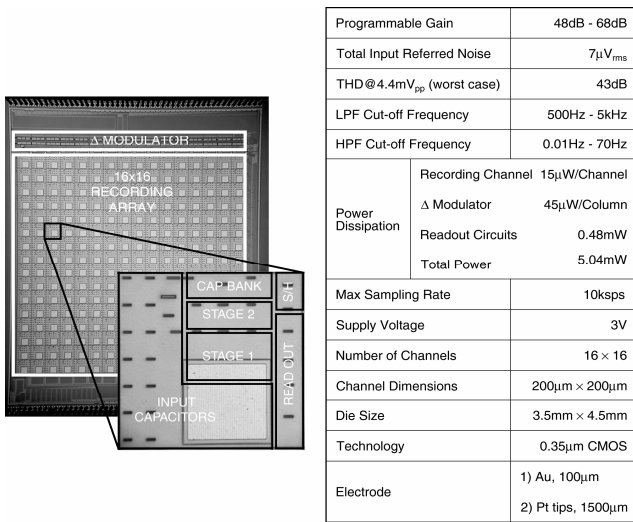


Figure 8.5.1: Chip micrograph and summary of experimentally measured characteristics.

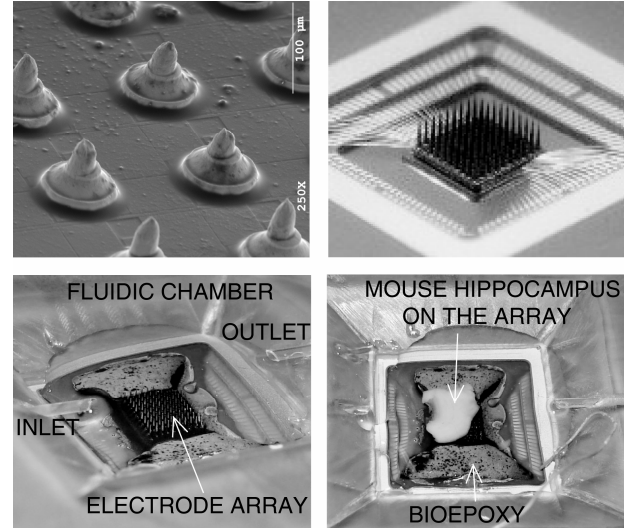


Figure 8.5.2: On-chip golden bump electrodes (top, left), Utah Electrode Array (top, right), and in vitro test setup (bottom).

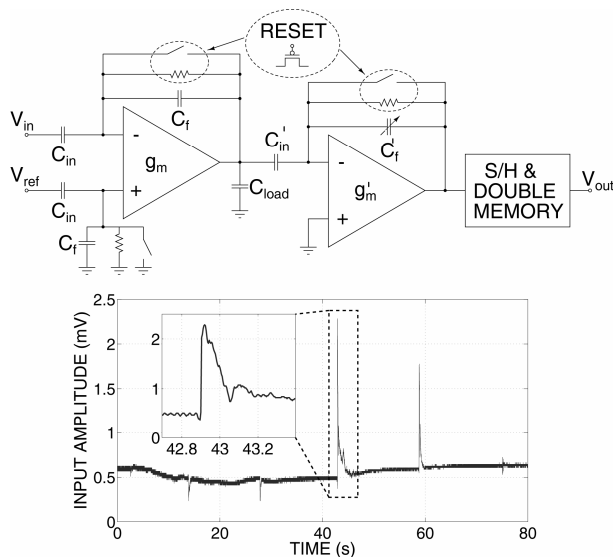


Figure 8.5.3: Channel block diagram and an experimental recording example.

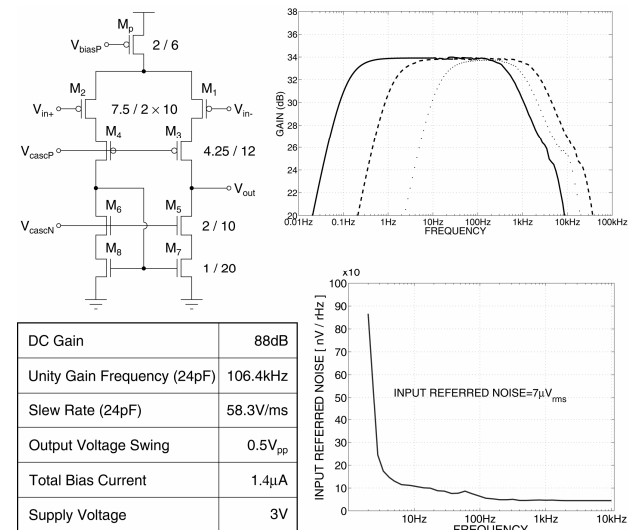


Figure 8.5.4: First stage circuit diagram and experimentally measured frequency response and noise.

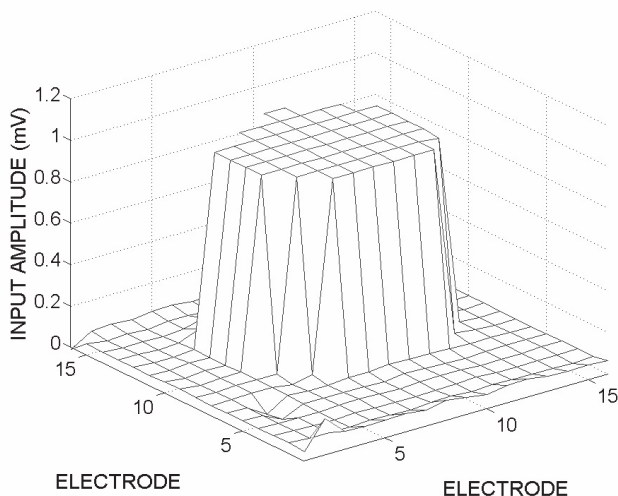


Figure 8.5.5: A two-dimensional experimental recording.

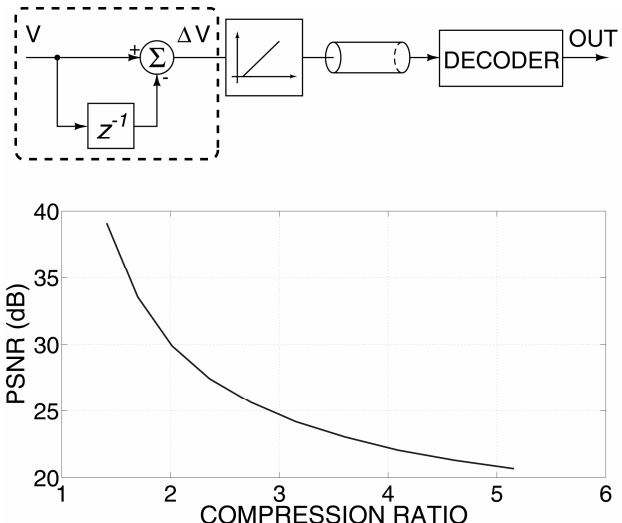


Figure 8.5.6: Delta compression encoder block diagram and simulated PSNR.

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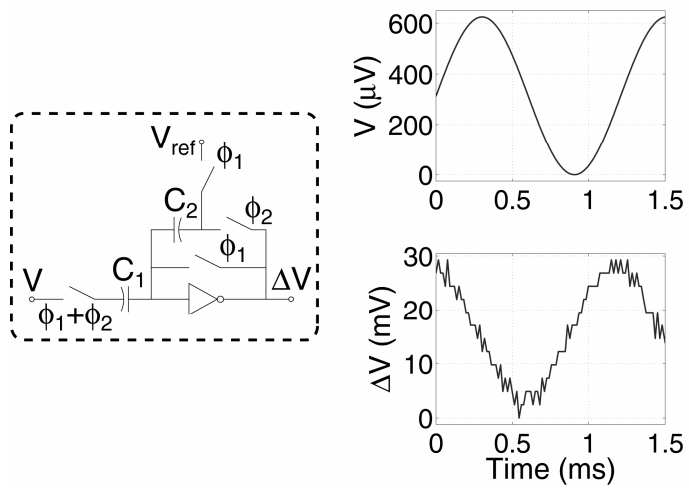


Figure 8.5.7: Delta-modulator circuit diagram and experimentally measured output waveform.